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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Dmitriy Rumynin et al.	Examiner:	David H. Malzahn
Serial No.:	09/637,532	Group Art Unit:	2124
Filed:	August 11, 2000	Docket:	1365.033US1
Title:	A PARALLEL COUNTER AND MULTIPLICATION LOGIC CIRCUIT		

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Supplemental Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

Pursuant to 37 C.F.R. §1.97(c)(2), Applicants have included the fee of \$180.00 as set forth in 37 C.F.R. §1.17(p). Please charge any additional fees or credit any overpayment to Deposit Account No. 19-0743.

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The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

DMITRIY RUMYNIN ET AL.

By their Representatives,

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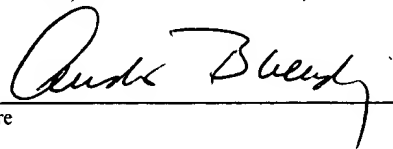
Date Sept. 15, 2004 By Ann M. McCrackin
Ann M. McCrackin
Reg. No. 42,858

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 15 day of September, 2004.

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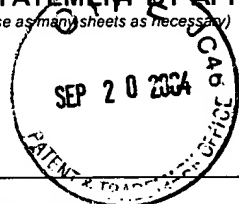


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Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)



Sheet 1 of 1

Complete if Known

Application Number	09/637,532
Filing Date	August 11, 2000
First Named Inventor	Rumynin, Dmitriy
Group Art Unit	2124
Examiner Name	Malzahn, David

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Attorney Docket No: 1365.033US1

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US PATENT DOCUMENTS

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
	US-5,978,827	11/02/1999	Ichikawa, T	708	709	04/10/1996

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T ²
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OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		BEDRIJ, O. J., "Carry-Select Adder", IRE Trans., EC-11, (June 1962),340-346	
		KNOWLES, S. , "A Family of Adders", Proc. 14th IEEE Symp. on Computer Arithmetic, (1999),30-34	
		KOGGE, P. M., et al., "A Parallel Algorithm for the Efficient Solution of a General Class of Recurrence Equations", IEEE Trans. Computers, Vol. C-22, No. 8, (Aug. 1973),786-793	
		LADNER, RICHARD E., et al., "Parallel Prefix Computation", Journal of ACM, Vol. 27, No. 4, (Oct. 1980),831-838	
		LING, HUEY , "High-Speed Binary Adder", IBM Journal of Research and Development, Vol. 25, No. 3, (1981),156-166	
		SKLANSKY, J. , "Conditional-Sum Addition Logic", IRE Trans., EC-9, (June 1960),226-231	
		WEINBERGER, A. , et al., "A Logic for High-Speed Addition", Nat. Bur. Stand. Circ., 591, (1958),3-12	

EXAMINER**DATE CONSIDERED**

Substitute Disclosure Statement Form (PTO-1449)

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached